AMENDMENTS TO THE SPECIFICATION

Please replace the following paragraphs beginning on page 2 through page 30 with the following amended paragraphs:

In accordance with the invention of a level shifter of ~~claim 1~~ a first embodiment, there is provided a level shifter for converting a signal level of a first logic circuit to which a first power source is supplied into a signal level of a second logic circuit to which a second power source is supplied, characterized by including a switching circuit between a GND power source terminal (ground power source terminal) of a level shift core circuit and a GND power source (ground power source), the switching circuit being controlled by a third logic circuit which generates control signals in accordance with control of the first power source, and a pull-up and/or pull-down circuit at an output of the level shift core circuit, the pull-up and/or pull-down circuit being controlled by the third logic circuit.

In accordance with the invention of a level shifter of ~~claim 2~~ a second embodiment, there is provided a level shifter for converting a signal level of a first logic circuit to which a first power source is supplied into a signal level of a second logic circuit to which a second power source is supplied, characterized by including a switching circuit between a power source terminal of a level shift core circuit and the second power source, the switching circuit being controlled by a third logic circuit which generates control signals in accordance with control of the first power source, and a pull-up and/or pull-down circuit at outputs of the level shift core circuit, the pull-up and/or pull-down circuit being controlled by the third logic circuit.

In accordance with the invention of a level shifter of ~~claim 3~~ a third embodiment, the level shifter in ~~claim 1 or 2~~ the first and second embodiments is characterized in that the level shift core circuit includes a p-MOS cross-coupled latch including at least two p-MOSs and a

differential n-MOS including at least two n-MOSs; each of the p-MOSs includes a source terminal connected to the second power source terminal and a gate terminal connected to a level shift output which is each drain terminal; and each of the n-MOSs includes a source terminal connected to the GND power source terminal, a drain terminal connected to the level shift output, and a gate terminal connected to a level shift input.

In accordance with the invention of a level shifter of ~~claim 4~~ a fourth embodiment, the level shifter in ~~claim 1 or 2~~ the first and second embodiments is characterized in that the level shift core circuit includes: a p-MOS cross-coupled latch including at least two p-MOSs each of which includes a source terminal connected to the second power source and a gate terminal connected to each level shift output; at least two p-MOSs switches in which a source terminal of the other p-MOS is connected to each drain terminal of the p-MOS, each gate terminal of the switches is connected to each level shift input, and each drain terminal of the switches is connected to the level shift output; and a differential n-MOS switch including at least two n-MOSs each of which includes a source terminal connected to the GND power source terminal, a drain terminal connected to the level shift output, and a gate terminal connected to a level shift input.

In accordance with the invention of a level shifter of ~~claim 5~~ a fifth embodiment, the level shifter in ~~claim 1 or 2~~ the first and second embodiments is characterized in that the pull-up and/or pull-down circuit is replaced with a pull-down circuit, the pull-down circuit including one n-MOS or at least two n-MOSs, each of the n-MOSs including a source connected to a GND power source, a gate terminal connected to an inverted signal of a control signal, and a drain terminal connected to at least one of the level shift outputs.

In accordance with the invention of a level shifter of ~~claim 6~~ a sixth embodiment, there is

provided a level shifter for converting a signal level of a first logic circuit to which a first power source is supplied into a signal level of a second logic circuit to which a second power source is supplied, characterized by including a pull-up and/or pull-down circuit in which the second power source is supplied to level shift outputs of a level shift core circuit, a control circuit to which the second power source is supplied and which receives as inputs thereto a level shift input signal and the level shift output signal, and a switching circuit which is disposed between a power source terminal of the level shift core circuit and the second power source and which is controlled by a third logic circuit, the third logic circuit generating control signals in accordance with control of the first power source, wherein the control circuit is controlled by a control signal from the third logic circuit.

In accordance with the invention of a level shifter of ~~claim 7~~ a seventh embodiment, the level shifter in ~~claim 6~~ the sixth embodiment is characterized in that the third logic circuit controls the control circuit by control signals from the third logic circuit, and the control circuit produces control signals to control the pull-up and/or pull-down circuit and the level shift core circuit.

In accordance with the invention of a level shifter of ~~claim 8~~ an eighth embodiment, the level shifter in ~~claim 5~~ the fifth embodiment is characterized in that the control circuit further produces control signals to control the pull-up and/or pull-down circuit to thereby control the pull-up and/or pull-down circuit.

In accordance with the invention of a level shifter of ~~claim 9~~ a ninth embodiment, the level shifter in ~~claim 1, 3, or 6~~ the first, third or sixth embodiments is characterized in that the pull-up and/or pull-down circuit includes at least two p-MOSs each of which including a source terminal connected to the second power source, a gate terminal connected to a control signal, and

a drain terminal connected to each of the level shift core outputs.

In accordance with the invention of a level shifter of ~~claim 10~~ a tenth embodiment, the level shifter in ~~claim 1, 3 or 8~~ the first, third or eighth embodiments is characterized in that the pull-up and/or pull-down circuit comprises a p-MOS including a source terminal connected to the second power source, a gate terminal connected to a control signal, and a drain terminal connected to one of the level shift outputs and an n-MOS including a source terminal connected to a GND power source, a gate terminal connected to an inverted signal of a control signal, and a drain terminal connected to other one of the level shift outputs.

In accordance with the invention of a level shifter of ~~claim 11~~ an eleventh embodiment, there is provided a level shifter for converting a signal level of a first logic circuit to which a first power source is supplied into a signal level of a second logic circuit to which a second power source is supplied, characterized by comprising a pull-down circuit at level shift output signals of a level shift core circuit and a control circuit to which the second power source is supplied and which receives as inputs thereto level shift input signals and the level shift output signals to produce control signals for the pull-down circuit and the level shift core circuit, wherein the control circuit and the pull-down circuit are controlled by control signals from the third logic circuit.

In accordance with the invention of a level shifter of ~~claim 12~~ a twelfth embodiment, the level shifter in ~~claim 11~~ the eleventh embodiment is characterized in that the NAND circuit is of a CMOS circuit configuration and the p-MOS transistor to which the level shift input signal is connected includes a transistor at least having a small ratio of a channel width/a channel length or a high threshold value.

In accordance with the invention of a level shifter of ~~claim 13~~ a thirteenth embodiment,

the level shifter in ~~claim 11~~ the eleventh embodiment is characterized in that the NAND circuit is of a CMOS circuit configuration and the n-MOS transistor to which a control signal output of the third logic circuit is connected includes a source terminal connected to a GND power source.

In accordance with the invention of a level shifter of ~~claim 14~~ a fourteenth embodiment, the level shifter in ~~claim 5~~ the fifth embodiment is characterized in that the pull-up and/or pull-down circuit includes at least two p-MOSs each of which includes a source terminal connected to the second power source and a gate terminal connected to a control signal from the control circuit, each drain terminal of other p-MOS being connected to each of the level shift outputs; at least two n-MOSs each of which includes a source terminal connected to the GND power source, a gate terminal connected to a control signal from the control circuit, and a drain terminal connected to the level shift outputs; and additionally at least two p-MOSs each of which includes a source terminal connected to the second power source and a gate terminal connected to a control signal from the third logic circuit, a drain terminal of other p-MOS being connected to each of the level shift outputs.

In accordance with the invention of a level shifter of ~~claim 15~~ a fifteenth embodiment, the level shifter in ~~claim 5~~ the fifth embodiment is characterized in that the pull-up and/or pull-down circuit includes at least two p-MOSs each of which includes a source terminal connected to the second power source and a gate terminal connected to a control signal from the control circuit, each drain terminal of other p-MOS being connected to each of the level shift outputs; at least two n-MOSs each of which includes a source terminal connected to the GND power source, a gate terminal connected to a control signal from the control circuit, and a drain terminal connected to the level shift outputs; and additionally a p-MOS including a source terminal connected to the second power source, a gate terminal connected to a control signal from the

third logic circuit, a drain terminal connected to one of the level shift outputs.

In accordance with the invention of a level shifter of ~~claim 16~~ a sixteenth embodiment, the level shifter in ~~claim 7~~ the seventh embodiment is characterized in that the pull-up and/or pull-down circuit includes at least two p-MOSs each of which includes a source terminal connected to the second power source, a gate terminal connected to a control signal from the control circuit, and a drain terminal connected to each of the level shift outputs; at least two n-MOSs each of which includes a source terminal connected to the GND power source, a gate terminal connected to a control signal from the control circuit, and a drain terminal connected to the level shift outputs; additionally a p-MOS including a source terminal connected to the second power source, a gate terminal connected to a control signal from the third logic circuit, and a drain terminal connected to one of the level shift outputs; and additionally an n-MOS including a source terminal connected to the GND power source, a gate terminal connected to a control signal from the third logic circuit or to an inverted signal of the control signal, and a drain terminal connected to other one of the level shift outputs.

In accordance with the invention of a level shifter of ~~claim 17~~ a seventeenth embodiment, the level shifter in ~~claim 5~~ the fifth embodiment is characterized in that the pull-up and/or pull-down circuit includes at least two p-MOSs each of which includes a source terminal connected to the second power source and a gate terminal connected to a control signal from the control circuit, a drain terminal of other p-MOS being connected to each of the level shift outputs; at least two n-MOSs each of which includes a source terminal connected to the GND power source, a gate terminal connected to a control signal from the control circuit, and a drain terminal connected to the level shift outputs; and additionally an n-MOS including a source terminal connected to the GND power source, a gate terminal connected to a control signal from the third

logic circuit or to an inverted signal of the control signal, and a drain terminal connected to one of the level shift outputs.

In accordance with the invention of a level shifter of ~~claim 18~~ an eighteenth embodiment, the level shifter in ~~claim 5~~ the fifth embodiment is characterized in that the control circuit comprises a NAND circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level shift input signal, an inverted signal of the level shift output signal, and a control output of the third logic circuit and a NAND circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level shift input signal, a positively inverted signal of the level shift output signal, and a control output of the third logic circuit, wherein an output signal of the NAND circuit is produced as a control signal.

In accordance with the invention of a level shifter of ~~claim 19~~ a nineteenth embodiment, the level shifter in ~~claim 18~~ the eighteenth embodiment is characterized in that the pull-up and/or pull-down circuit further includes at least two p-MOSs each of which includes a source terminal connected to the second power source and a gate terminal connected to a control signal from the control circuit, a drain terminal of other p-MOS being connected to each of the level shift outputs; and additionally at least two p-MOSs each of which includes a source terminal connected to the second power source and a gate terminal connected to a control signal from the third logic circuit, a drain terminal of other p-MOS being connected to each of the level shift outputs.

In accordance with the invention of a level shifter of ~~claim 20~~ a twentieth embodiment, the level shifter in ~~claim 18~~ the eighteenth embodiment is characterized in that the pull-up and/or pull-down circuit further includes at least two p-MOSs each of which includes a source terminal

connected to the second power source, a gate terminal connected to a control signal from the control circuit, and a drain terminal connected to each of the level shift outputs; and additionally a p-MOS including a source terminal connected to the second power source, a gate terminal connected to a control signal from the third logic circuit, and a drain terminal connected to one of the level shift outputs.

In accordance with the invention of ~~claim 21~~ a level shifter of a twenty-first embodiment, the level shifter in ~~claim 18~~ the eighteenth embodiment is characterized in that the pull-up and/or pull-down circuit includes at least two p-MOSs each of which includes a source terminal connected to the second power source, a gate terminal connected to a control signal from the control circuit, and a drain terminal connected to each of the level shift outputs; additionally a p-MOS including a source terminal connected to the second power source, a gate terminal connected to a control signal from the third logic circuit, and a drain terminal connected to one of the level shift outputs; and additionally an n-MOS including a source terminal connected to the GND power source, a gate terminal connected to a control signal from the third logic circuit or to an inverted signal of the control signal, and a drain terminal connected to other one of the level shift outputs.

In accordance with the invention of a level shifter of ~~claim 22~~ a twenty-second embodiment, the level shifter in ~~claim 18~~ the eighteenth embodiment is characterized in that the pull-up and/or pull-down circuit includes at least two p-MOSs each of which includes a source terminal connected to the second power source, a gate terminal connected to a control signal from the control circuit, and a drain terminal connected to each of the level shift outputs; and additionally an n-MOS including a source terminal connected to the GND power source, a gate terminal connected to a control signal from the third logic circuit or an inverted signal of the

control signal, and a drain terminal connected to one of the level shift outputs.

In accordance with the invention of a level shifter of ~~claim 23~~ a twenty-third embodiment, the level shifter in ~~claim 5~~ the fifth embodiment is characterized in that the control circuit comprises a NAND circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level shift input signal, an inverted signal of the level shift output signal, and a control output of the third logic circuit, a NAND circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level shift input signal, a positively inverted signal of the level shift output, and a control output of the third logic circuit, and at least two inverters to which the second power source is supplied and which respectively receive as inputs thereto outputs from the NAND circuits, wherein each output signal from the inverters is produced as a control signal.

In accordance with the invention of a level shifter of ~~claim 24~~ a twenty-fourth embodiment, the level shifter in ~~claim 18~~ the eighteenth embodiment is characterized in that the pull-up and/or pull-down circuit includes at least two n-MOSs each of which includes a source terminal connected to the GND power source, a gate terminal connected to a control signal from the control circuit, and a drain terminal connected to the level shift outputs and additionally at least two p-MOSs each of which includes a source terminal connected to the second power source and a gate terminal connected to a control signal from the third logic circuit, a drain terminal of other p-MOS being connected to each of the level shift outputs.

In accordance with the invention of a level shifter of ~~claim 25~~ a twenty-fifth embodiment, the level shifter in ~~claim 23~~ the twenty-third embodiment is characterized in that the pull-up and/or pull-down circuit includes at least two n-MOSs each of which includes a source terminal connected to the GND power source, a gate terminal connected to a control signal from the

control circuit, and a drain terminal connected to the level shift outputs and additionally a p-MOS including a source terminal connected to the second power source, a gate terminal connected to a control signal from the third logic circuit, and a drain terminal connected to one of the level shift outputs.

In accordance with the invention of a level shifter of ~~claim 26~~ a twenty-sixth embodiment, the level shifter in ~~claim 23~~ the twenty-third embodiment is characterized in that the pull-up and/or pull-down circuit includes at least two n-MOSs each of which includes a source terminal connected to the GND power source, a gate terminal connected to a control signal from the control circuit, and a drain terminal connected to the level shift outputs; additionally a p-MOS including a source terminal connected to the second power source, a gate terminal connected to a control signal from the third logic circuit, and a drain terminal connected to one of the level shift outputs; and additionally an n-MOS including a source terminal connected to the GND power source, a gate terminal connected to a control signal from the third logic circuit or an inverted signal of the control signal, and a drain terminal connected to other one of the level shift outputs.

In accordance with the invention of a level shifter of ~~claim 27~~ a twenty-seventh embodiment, the level shifter in ~~claim 23~~ the twenty-third embodiment is characterized in that the pull-up and/or pull-down circuit includes at least two n-MOSs each of which includes a source terminal connected to the GND power source, a gate terminal connected to a control signal from the control circuit, and a drain terminal connected to the level shift outputs and additionally an n-MOS including a source terminal connected to the GND power source, a gate terminal connected to a control signal from the third logic circuit or to an inverted signal of the control signal, and a drain terminal connected to other one of the level shift outputs.

In accordance with the invention of a level shifter of ~~claim 28~~ a twenty-eighth embodiment, the level shifter in ~~claims 14 to 17~~ the fourteenth to seventeenth embodiments is characterized in that the control circuit comprises a NOR circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level shift input signal, a positively inverted signal of the level shift output signal, and a control output of the third logic circuit or an inverted signal of the control output, a NOR circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level shift input signal, an inverted signal of the level shift output, and a control output of the third logic circuit or an inverted signal of the control output, and at least two inverters to which the second power source is supplied and which respectively receive as inputs thereto outputs from the NOR circuits, wherein output signals respectively from the at least two NOR circuits and the at least two inverters are produced as control signals.

In accordance with the invention of a level shifter of ~~claim 29~~ a twenty-ninth embodiment, the level shifter in ~~claim 28~~ the twenty-eighth embodiment is characterized in that the NOR circuits are of a CMOS circuit configuration and a p-MOS to which the level shift input signal is connected includes a transistor at least having a small ratio of a channel width/a channel length or a threshold value which is of a negative polarity and which is a large absolute value.

In accordance with the invention of a level shifter of ~~claim 30~~ a thirtieth embodiment, the level shifter in ~~claim 28~~ the twenty-eighth embodiment is characterized in that the NOR circuits are of a CMOS circuit configuration and a control signal from the third logic circuit or an inverted signal thereof is connected to a p-MOS on a power source side.

In accordance with the invention of a level shifter of ~~claim 31~~ a thirty-first embodiment, the level shifter in ~~claims 19 to 22~~ the nineteenth to twenty-second embodiments is characterized

in that the control circuit comprises a NOR circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level shift input signal, a positively inverted signal of the level shift output signal, and a control output of the third logic circuit or an inverted signal of the control output, a NOR circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level shift input signal, an inverted signal of the level shift output, and a control output of the third logic circuit or an inverted signal of the control output, and at least two inverters to which the second power source is supplied and which receive as inputs thereto outputs from the respective NOR circuits, wherein each output signal from the inverters is produced as a control signal.

In accordance with the invention of a level shifter of ~~claim 32~~ a thirty-second embodiment, the level shifter in ~~claims 24 to 27~~ the twenty-fourth to twenty-seventh embodiments is characterized in that the control circuit comprises a first NOR circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level shift input signal, a positively inverted signal of the level shift output signal, and a control output of the third logic circuit or an inverted signal of the control output and a second NOR circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level shift input signal, an inverted signal of the level shift output, and a control output of the third logic circuit or an inverted signal of the control output, wherein each output signal from the first and second NOR circuits is produced as a control signal.

In accordance with the invention of a level shifter of ~~claim 33~~ a thirty-third embodiment, the level shifter in ~~claim 6~~ the sixth embodiment is characterized in that the control circuit comprises an AND-NOR circuit to which the second power source is supplied and which

receives as inputs thereto a positively inverted signal of the level shift input signal, an inverted signal of the level shift output signal, and a control output of the third logic circuit or an inverted signal of the control output, a NAND circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level shift input signal, a positively inverted signal of the level shift output, and a control output of the third logic circuit, and at least two inverters to which the second power source is supplied and which receive as inputs thereto outputs from the respective NAND circuits, wherein output signals from the AND-NOR circuit, the NAND circuit, and the inverters are produced as control signals.

In accordance with the invention of a level shifter of ~~claim 34~~ a thirty-fourth embodiment, the level shifter in ~~claim 6 or 8~~ the sixth and eighth embodiments is characterized in that the pull-up and/or pull-down circuit includes at least two p-MOSs each of which includes a source terminal connected to the second power source and a gate terminal connected to a control signal from the control circuit, a drain terminal of other p-MOS being connected to each of the level shift outputs and at least two n-MOSs each of which includes a source terminal connected to the GND power source, a gate terminal connected to a control signal from the control circuit, and a drain terminal connected to the level shift outputs.

In accordance with the invention of a level shifter of ~~claim 35~~ a thirty-fifth embodiment, the level shifter in ~~claim 6~~ the sixth embodiment is characterized in that the control circuit comprises an AND-NOR circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level shift input signal, an inverted signal of the level shift output signal, and a control output of the third logic circuit or an inverted signal of the control output and a NAND circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level shift input signal, a positively

inverted signal of the level shift output, and a control output of the third logic circuit, wherein respective output signals from the AND-NOR circuit and the NAND circuit are produced as control signals.

In accordance with the invention of a level shifter of ~~claim 36~~ a thirty-sixth embodiment, the level shifter in ~~claim 35~~ the thirty-fifth embodiment is characterized in that the pull-up and/or pull-down circuit includes at least two p-MOSs each of which includes a source terminal connected to the second power source and a gate terminal connected to a control signal from the control circuit, a drain terminal of other p-MOS being connected to each of the level shift outputs.

In accordance with the invention of a level shifter of ~~claim 37~~ the thirty-seventh embodiment, the level shifter in ~~claim 6~~ the sixth embodiment is characterized in that the control circuit comprises an AND-NOR circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level shift input signal, an inverted signal of the level shift output signal, and a control output of the third logic circuit or an inverted signal of the control output, a NAND circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level shift input signal, a positively inverted signal of the level shift output, and a control output of the third logic circuit, and at least two inverters to which the second power source is supplied and which receive as inputs thereto outputs from the respective NAND circuits, wherein each output signal from the inverters is produced as a control signal.

In accordance with the invention of a level shifter of ~~claim 38~~ a thirty-eighth embodiment, the level shifter in ~~claim 37~~ the thirty-seventh embodiment is characterized in that the pull-up and/or pull-down circuit includes at least two n-MOSs each of which includes a

source terminal connected to the GND power source, a gate terminal connected to a control signal from the control circuit, and a drain terminal connected to the level shift outputs.

In accordance with the invention of a level shifter of ~~claim 39~~ a thirty-ninth embodiment, the level shifter in ~~claim 34~~ the thirty-fourth embodiment is characterized in that the control circuit comprises an OR-NAND circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level shift input signal, a positively inverted signal of the level shift output signal, and a control output of the third logic circuit, a NOR circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level shift input signal, an inverted signal of the level shift output, and a control output of the third logic circuit or an inverted signal of the control output, and at least two inverters to which the second power source is supplied and which receive as inputs thereto outputs from the each of the NOR circuits, wherein each output signal from the OR-NAND circuit, the NOR circuits, and the inverters is produced as a control signal.

In accordance with the invention of a level shifter of ~~claim 40~~ a fortieth embodiment, the level shifter in ~~claim 39~~ the thirty-ninth embodiment is characterized in that the OR-NAND circuit is of a CMOS circuit configuration and a p-MOS to which the level shift input signal is connected has at least one condition that the p-MOS has a small ratio of a channel width/a channel length or a threshold value which is of a negative polarity and which is a large absolute value.

In accordance with the invention of a level shifter of ~~claim 41~~ a forty-first embodiment, the level shifter in ~~claim 39~~ the thirty-ninth embodiment is characterized in that the OR-NAND circuit is of a CMOS circuit configuration and a control signal from the third logic circuit is connected to an n-MOS on a GND power source side.

In accordance with the invention of a level shifter of ~~claim 42~~ a forty-second embodiment, the level shifter in ~~claim 36~~ the thirty-sixth embodiment is characterized in that the control circuit comprises an OR-NAND circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level shift input signal, a positively inverted signal of the level shift output signal, and a control output of the third logic circuit, a NOR circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level shift input signal, an inverted signal of the level shift output, and a control output of the third logic circuit or an inverted signal of the control output, and at least two inverters to which the second power source is supplied and which receive as inputs thereto outputs from the respective NOR circuits, wherein each output signal from the inverters is produced as a control signal.

In accordance with the invention of a level shifter of ~~claim 43~~ a forty-third embodiment, the level shifter in ~~claim 38~~ the thirty-eighth embodiment is characterized in that the control circuit comprises an OR-NAND circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level shift input signal, a positively inverted signal of the level shift output signal, and a control output of the third logic circuit and a NOR circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level shift input signal, an inverted signal of the level shift output, and a control output of the third logic circuit or an inverted signal of the control output, wherein each output signal from the OR-NAND circuit and the NOR circuit is produced as a control signal.

In accordance with the invention of a level shifter of ~~claim 44~~ a forty-fourth embodiment, the level shifter in ~~claim 36~~ the thirty-sixth embodiment is characterized in that the control

circuit comprises an AND-NOR circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level shift input signal, an inverted signal of the level shift output signal, and a control output of the third logic circuit or an inverted signal of the control output and an AND-NOR circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level shift input signal, a positively inverted signal of the level shift output, and a control output of the third logic circuit or an inverted signal of the control output, wherein each output signal from the AND-NOR circuits is produced as a control signal.

In accordance with the invention of a level shifter of ~~claim 45~~ a forty-fifth embodiment, the level shifter in ~~claim 36~~ the thirty-sixth embodiment is characterized in that the control circuit comprises an OR-NAND circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level shift input signal, a positively inverted signal of the level shift output signal, and a control output of the third logic circuit, an OR-NAND circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level shift input signal, an inverted signal of the level shift output, and a control output of the third logic circuit, and at least two inverters to which the second power source is supplied and which receive as inputs thereto outputs from the respective OR-NAND circuits, wherein each output signal from the inverters is produced as a control signal.

In accordance with the invention of a level shifter of ~~claim 46~~ a forty-sixth embodiment, the level shifter in ~~claim 38~~ the thirty-eighth embodiment is characterized in that the control circuit comprises an AND-NOR circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level shift input signal, an inverted

signal of the level shift output signal, and a control output of the third logic circuit or an inverted signal of the control output, an AND-NOR circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level shift input signal, a positively inverted signal of the level shift output, and a control output of the third logic circuit or an inverted signal of the control output, and at least two inverters to which the second power source is supplied and which receive as inputs thereto outputs from the respective AND-NOR circuits, wherein each output signal from the inverters is produced as a control signal.

In accordance with the invention of a level shifter of ~~claim 47~~ a forty-seventh embodiment, the level shifter in ~~claim 38~~ the thirty-eighth embodiment is characterized in that the control circuit comprises an OR-NAND circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level shift input signal, a positively inverted signal of the level shift output signal, and a control output of the third logic circuit and an OR-NAND circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level shift input signal, an inverted signal of the level shift output, and a control output of the third logic circuit, wherein each output signal from the OR-NAND circuits is produced as a control signal.

In accordance with the invention of a level shifter of ~~claim 48~~ a forty-eighth embodiment, the level shifter in ~~claim 47~~ the forty-seventh embodiment is characterized in that the level shift core circuit comprises a p-MOS cross-coupled latch including at least two of the p-MOS in which each source terminal is connected to the second source and a gate terminal of other p-MOS is connected to each of the level shift outputs, at least two p-MOS switches including a source terminal connected of a drain terminal of the p-MOS, each gate terminal connected to a control signal from the control circuit, and each drain terminal connected to the level shift

outputs, and a differential n-MOS switch including at least two n-MOSs each of which includes a source terminal connected to a GND power source, a drain terminal connected to the respective level shift outputs, and a gate terminal connected to a level shift input.

In accordance with the invention of a level shifter of ~~claim 49~~ a forty-ninth embodiment, the level shifter in claim one of ~~claims 14 to 17, 19 to 22, and 24 to 27~~ the fourteenth to seventeenth, nineteenth to twenty-second, and twenty-fourth to twenty-seventh embodiments, characterized in that the control circuit comprises a first NAND circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level shift input signal, an inverted signal of the level shift output signal, and a control output of the third logic circuit, a second NAND circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level shift input signal, a positively inverted signal of the level shift output, and a control output of the third logic circuit, and at least two inverters to which the second power source is supplied and which receive as inputs thereto outputs from the respective NAND circuits, wherein each output signal from the first and second NAND circuits and the at least two inverters is produced as a pull-up and/or pull-down control signal and each output signal of the inverters is produced as a control signal of the level shift core circuit.

In accordance with the invention of a level shifter of claim 50 a fiftieth embodiment, the level shifter in one of ~~claims 14 to 17, 19 to 22, and 24 to 27~~ the fourteenth to seventeenth, nineteenth to twenty-second and twenty-fourth to twenty-seventh embodiments, characterized in that the control circuit comprises a NOR circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level shift input signal, a positively inverted signal of the level shift output signal, and a control output of the third logic circuit or an

inverted signal of the control output, a NOR circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level shift input signal, an inverted signal of the level shift output, and a control output of the third logic circuit or an inverted signal of the control output, and at least two inverters to which the second power source is supplied and which respectively receive as inputs thereto outputs from the respective NOR circuits, wherein each output signal from the NOR circuits and the inverters is produced as a pull-up and/or pull-down control signal and each output signal of the NOR circuits is produced as a control signal of the level shift core circuit.

In accordance with the invention of a level shifter of ~~claim 51~~ a fifty-first embodiment, the level shifter in claim one of ~~claims 1, 3, and 6 to 9~~ the first, third and sixth to the ninth embodiments characterized in that the switching circuit comprises an n-MOS including a source terminal connected to a GND power source, a gate terminal connected to a control signal, and a drain terminal connected to a GND power source terminal of the level shift core circuit.

In accordance with the invention of a level shifter of ~~claim 52~~ a fifty-second embodiment, the level shifter in ~~claim 34~~ the thirty-fourth embodiment, characterized in that the control circuit comprises an AND-NOR circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level shift input signal, an inverted signal of the level shift output signal, and a control output of the third logic circuit or an inverted signal of the control output, a NAND circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level shift input signal, a positively inverted signal of the level shift output, and a control output of the third logic circuit, and at least two inverters to which the second power source is supplied and which receive as inputs thereto outputs from the respective NAND circuits, wherein each output signal from the AND-NOR

circuit, the NAND circuit, and the at least two inverters is produced as a pull-up and/or pull-down control signal and each output signal of the inverters is produced as a control signal of the level shift core circuit.

In accordance with the invention of a level shifter of ~~claim 53~~ a fifty-third embodiment, the level shifter in ~~claim 39~~ the thirty-ninth embodiment, characterized in that each output signal from the OR-NAND circuit, the NOR circuit, and the inverters is produced as a pull-up and/or pull-down control signal and each output signal of the OR-NAND circuit and the NOR circuit is produced as a control signal of the level shift core circuit.

In accordance with the invention of a level shifter of ~~claim 54~~ a fifty-fourth embodiment, the level shifter in ~~claim 8~~ the eighth embodiment, characterized in that the control circuit comprises a first AND-NOR circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level shift input signal, an inverted signal of the level shift output signal, and a control output of the third logic circuit or an inverted signal of the control output, a second AND-NOR circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level shift input signal, a positively inverted signal of the level shift output, and a control output of the third logic circuit or an inverted signal of the control output, and at least two inverters to which the second power source is supplied and which receive as inputs thereto outputs from the first and second AND-NOR circuits, wherein each output signal from the first and second AND-NOR circuits is produced as a pull-up and/or pull-down control signal and each output signal of the inverters is produced as a control signal of the level shift core circuit, and the pull-up and/or pull-down circuit includes at least two p-MOSs each of which includes a source terminal connected to the second power source and a gate terminal connected to a control signal from the control circuit, a

drain terminal of other p-MOS being connected to each of the level shift outputs.

In accordance with the invention of a level shifter of ~~claim 55~~ a fifty-fifth embodiment, the level shifter in ~~claim 8~~ the eighth embodiment, characterized in that the control circuit comprises a first OR-NAND circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level shift input signal, a positively inverted signal of the level shift output signal, and a control output of the third logic circuit, a second OR-NAND circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level shift input signal, an inverted signal of the level shift output, and a control output of the third logic circuit, and at least two inverters to which the second power source is supplied and which receive as inputs thereto outputs from the first and second OR-NAND circuits, wherein each output signal from the at least two inverters is produced as a pull-up and/or pull-down control signal and each output signal from the OR-NAND circuits is produced as a control signal of the level shift core circuit, and the pull-up and/or pull-down circuit includes at least two p-MOSs each of which includes a source terminal connected to the second power source and a gate terminal connected to a control signal from the control circuit, a drain terminal of other p-MOS being connected to each of the level shift outputs.

In accordance with the invention of a level shifter of ~~claim 56~~ a fifty-sixth embodiment, the level shifter in one of ~~claim 4 to 7 and 9 to 11~~ the fourth to seventh and ninth to eleventh embodiments, characterized in that the control circuit comprises an AND-NOR circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level shift input signal, an inverted signal of the level shift output signal, and a control output of the third logic circuit or an inverted signal of the control output, an AND-NOR

circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level shift input signal, a positively inverted signal of the level shift output, and a control output of the third logic circuit or an inverted signal of the control output, and at least two inverters to which the second power source is supplied and which receive as inputs thereto outputs from the respective AND-NOR circuits, wherein each output signal from the inverters is produced as a pull-up and/or pull-down control signal, each output signal from the inverters is produced as a control signal of the level shift core circuit, and the pull-up and/or pull-down circuit includes at least two n-MOS each of which includes a source terminal connected to the GND power source, a gate terminal connected to a control signal from the control circuit, and a drain terminal connected to the level shift outputs.

In accordance with the invention of a level shifter of ~~claim 57~~ a fifty-seventh embodiment, the level shifter in one of ~~claims 4 to 7 and 9 to 11~~ the fourth to seventh and ninth to eleventh embodiments, characterized in that the control circuit comprises a first OR-NAND circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level shift input signal, a positively inverted signal of the level shift output signal, and a control output of the third logic circuit and a second OR-NAND circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level shift input signal, an inverted signal of the level shift output, and a control output of the third logic circuit, wherein each output signal from the first and second OR-NAND circuits is produced as a pull-up and/or pull-down control signal, each output signal from the OR-NAND circuits is produced as a control signal of the level shift core circuit, and the pull-up and/or pull-down circuit includes at least two n-MOSs each of which includes a source terminal connected to the GND power source, a gate terminal connected to a control signal from the control circuit, and

a drain terminal connected to the level shift outputs.

In accordance with the invention of a level shifter of ~~claim 58~~ a fifty-eighth embodiment, the level shifter in one of ~~claims 4 to 7 and 9 to 11~~ the fourth to seventh and ninth to eleventh embodiments, characterized in that the control circuit comprises an AND-NOR circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level shift input signal, an inverted signal of the level shift output signal, and a control output of the third logic circuit or an inverted signal of the control output, an AND-NOR circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level shift input signal, a positively inverted signal of the level shift output, and a control output of the third logic circuit or an inverted signal of the control output, and at least two inverters to which the second power source is supplied and which receive as inputs thereto outputs from the respective AND-NOR circuits, wherein each output signal of the inverters is produced as a control signal of the level shift core circuit.

In accordance with the invention of a level shifter of claim 59 a fifty-ninth embodiment, the level shifter in one of ~~claims 4 to 7 and 9 to 11~~ the fourth to seventh and ninth to eleventh embodiments, characterized in that the control circuit comprises an OR-NAND circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level shift input signal, a positively inverted signal of the level shift output signal, and a control output of the third logic circuit and an OR-NAND circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level shift input signal, an inverted signal of the level shift output, and a control output of the third logic circuit, wherein each output signal from the OR-NAND circuits is produced as a control signal of the level shift core circuit.

In accordance with the invention of a level shifter of ~~claim 60~~ *a sixtieth embodiment*, the level shifter in one of ~~claims 1, 3, 10, 59 and 60~~ the first, third, tenth, fifty-ninth and the sixtieth embodiments, characterized in that: the level shift core circuit comprises a p-MOS cross-coupled latch including at least two first p-MOS, a differential n-MOS including at least two n-MOSs, and at least two second p-MOS, wherein: the p-MOS cross-coupled latch includes a source terminal connected to the second power source and a gate terminal connected to a level shift output which is each drain terminal; the differential n-MOS includes each source terminal connected to the GND power source, each drain terminal connected to the level shift output, and each gate terminal connected to a level shift input; and the second p-MOS includes each drain terminal connected to the second power source, each gate terminal connected to the level shift input, and each source terminal connected to the level shift output.

In accordance with the invention of a level shifter of ~~claim 61~~ a sixty-first embodiment, there is provided a level shifter for converting a signal level of a first logic circuit to which a first power source is supplied into a signal level of a second logic circuit to which a second power source is supplied, characterized by including a pull-down circuit at level shift outputs of a level shift core circuit and a control circuit to which the second power source is supplied and which receives as inputs thereto level shift input signals and the level shift output signals to produce control signals for a pull-down circuit and a level shift core circuit, wherein the control circuit is also connected to control signals from the third logic circuit.

In accordance with the invention of a level shifter of ~~claim 62~~ a sixty-second embodiment, the level shifter in ~~claim 61~~ the sixty-first embodiment, characterized in that the control circuit, the control circuit comprises a first OR-NAND circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level shift input

signal, a positively inverted signal of the level shift output signal, and a control output of the third logic circuit and a second OR-NAND circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level shift input signal, an inverted signal of the level shift output, and a control output of the third logic circuit, wherein each output signal from the first and second OR-NAND circuits is produced as a pull-up and/or pull-down control signal, each output signal from the OR-NAND circuits is produced as a control signal of the level shift core circuit, and the pull-down circuit, the pull-up and/or pull-down circuit include at least two n-MOSs each of which includes a source terminal connected to the GND power source, a gate terminal connected to a control signal from the control circuit, and a drain terminal connected to the level shift outputs.

In accordance with the invention of a level shifter of ~~claim 63~~ a sixty-third embodiment, the level shifter in ~~claim 61~~ the sixty-first embodiment, characterized in that the control circuit, the control circuit comprises a first OR-NAND circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level shift input signal, a positively inverted signal of the level shift output signal, and a control output of the third logic circuit and a second OR-NAND circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level shift input signal, an inverted signal of the level shift output, and a control output of the third logic circuit or an inverted signal of the control output, wherein each output signal from the first and second OR-NAND circuits is produced as a pull-up and/or pull-down control signal, each output signal from the OR-NAND circuits is produced as a control signal of the level shift core circuit, and the pull-down circuit, the pull-up and/or pull-down circuit include at least two n-MOSs each of which includes a source terminal connected to the GND power source, a gate terminal connected to a control signal from

the control circuit, and a drain terminal connected to the level shift outputs.

In accordance with the invention of a level shifter of ~~claim 64~~ a sixty-fourth embodiment, the level shifter in one of ~~claims 2, 7 to 9, and 61~~ the second, seventh to the ninth and sixty-first embodiments, characterized in that the switching circuit comprises a p-MOS including a source terminal connected to the second power source, a gate terminal connected to a control signal or an inverted signal thereof, and a drain terminal connected to a power source terminal of the level shift core circuit.

In accordance with the invention of a level shifter of ~~claim 65~~ a sixty-fifth embodiment, the level shifter in one of ~~claims 3, 5, 6 and 61~~ the third, fifth, sixth and sixty-first embodiments, characterized in that the control circuit comprises at least two NOR circuits to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level shift input signal, a positively inverted signal of the level shift output signal, and a control output of the third logic circuit or an inverted signal of the control output and a NOR circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level shift input signal, an inverted signal of the level shift output, and a control output of the third logic circuit or an inverted signal of the control output, wherein each output signal from the NOR circuits is produced as a control signal of the level shift core circuit.

In accordance with the invention of a level shifter of ~~claim 66~~ a sixty-sixth embodiment, the level shifter in one of ~~claims 3, 11, 12, and 61~~ the third, eleventh, twelfth and sixty-first embodiments, characterized in that the control circuit comprises at least two NAND circuits to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level shift input signal, an inverted signal of the level shift output signal, and a control output of the third logic circuit, a NAND circuit to which the second

power source is supplied and which receives as inputs thereto an inverted signal of the level shift input signal, a positively inverted signal of the level shift output signal, and a control output of the third logic circuit, and at least two inverters to which the second power source is supplied and which receives as inputs thereto outputs from the respective NAND circuits, wherein each output signal from the inverters is produced as a control signal of the level shift core circuit.

Please delete the present Abstract of the Disclosure.

Please add the following new Abstract of the Disclosure:

~~There is provided a~~ A level shifter in which short circuit current and the increase in delay are reduced when a ~~firth~~ first power source is controlled. In a level shifter for converting a signal level of a first logic circuit to which a first power source is supplied into a signal level of a second logic circuit to which a second power source is supplied, the circuit ~~has a configuration characterized by including~~ includes a switching circuit between a GND power source terminal of a level shift core circuit and a GND power source~~,~~. The switching circuit ~~being~~ is controlled by a third logic circuit which generates a control signal under control of the first power source, and a pull-up/pull-down circuit at an output of the level shift core circuit~~,~~. The pull-up and/or pull-down circuit ~~being~~ is controlled by the third logic circuit.